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Design and implementation of a platform for experimental testing and validation of analog-to-digital converters: static and dynamic parameters

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Abstract. This paper presents an implementation of a data acquisition system for analog-to-digital converters (ADCs) using "Laboratory Virtual Instrument Engineering Workbench (LabVIEW)" as software for data analysis. The designed and implemented platform allows interaction with the device under test through means of data acquisition and instrument controls. Developing custom tests in LabVIEW can result in reduced test time, which in turn will help reduce costs in testing. This system was developed for evaluation purposes of ADC's static and dynamic parameters (gain error, offset error, DNL, INL, SNR, SINAD, IMD, etc.) using single and multi-frequency signals. The virtual control and analysis instrument was created in "LabVIEW" environment to control test signals generation and data acquisition. The testing performance of the platform is demonstrated using the classical ADC circuit "ADC0804". A comparison with experimental results obtained by CANTEST platform from Bordeaux University (France) is also presented to highlight our platform.

Keywords: analog-to-digital converter / static and dynamic specifications / spectral analysis / LabVIEW environment / testing and validation

1 Introduction

Analog-to-digital converters (ADCs) are nowadays part of complex systems developed for various applications such as medical applications, telecommunications, and consumer applications [1]. They translate analog electrical signals representing real-world: light, sound, temperature or pressure to binary numbers. It is an electronic system or a module that has analog input, reference voltage input and digital outputs. The ADC converts analog input signal to digital output values (bits) that represent the size of the analog input comparing to the reference voltage, as shown in Figure 1. The input/output transfer function of an ADC is given by the following formula:

$$\text{Output} = 2^N \times G \times \frac{V_{\text{in}}}{V_{\text{ref}}}, \tag{1}$$

where N is the number of output bits (resolution), G is the gain factor (usually "1"), V_{in} is the analog input voltage (or current), V_{ref} is the reference voltage (or current).

There is a wide variety of ADC architectures available depending on the requirements of the application. ADCs performances vary from high-speed, low resolution (example: flash converters) to high-resolution, low-bandwidth over-sampled noise-shaping (example: sigma delta converters).

The high-sample rates required for serial link applications can be attained in two ways. First, a single-channel high speed ADC can be used, which limits the choice of architectures available. The alternative solution is to use several lower sample-rate ADCs in a time-interleaved configuration, in order to increase the sample-rate. This allows a variety of architectures to be used depending on the specific requirements such as power dissipation, area, latency and design time [2]. The architectures that are used for high-sample rate applications, either in a single-channel or time-interleaved are: flash ADCs, folding ADCs, pipeline ADCs and successive approximation ADCs. In this work, we are interested in successive approximation architecture which represents the majority of the ADC market for medium to high resolution ADCs.

The successive approximation ADC can be seen as the implementation of a binary search algorithm. In a single stage, the input is sampled and then a state-machine

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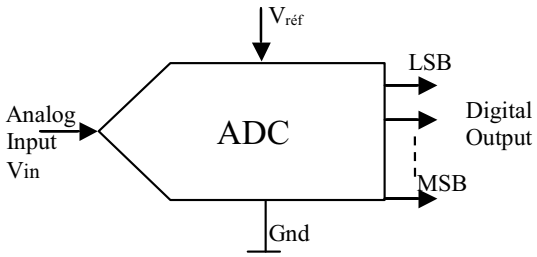

Fig. 1. Basic diagram of ADC [13].

controls a digital-to-analog converter (DAC) output, determining one by one, the bits from the most significant bit (MSB) to the least significant bit (LSB). As the search algorithm is iterative, only one comparator is needed. The comparator output sequentially updates the successive approximation register (SAR). The input signal is sampled at the beginning of the conversion and after "*k*" clock cycles the conversion is complete and a new sample is taken. Therefore, the sampling frequency is less than the internal clock frequency. This is a major disadvantage of the SAR ADC architecture [2].

At present, most part of the signal processing in areas like instrumentation, telecommunications, control and consumer electronics is carried out at the digital level. The role of ADCs placed at the borders of the digital domain is getting a particular relevance, since the signal degradation introduced by these components cannot normally be recovered by subsequent processing. The correct evaluation of the whole system performance therefore requires the test of these mixed-signal devices [3]. There are various methods of finding the code edges of an ADC such as binary search methods that are well-suited for production testing of circuits that are essentially one-bit ADCs like comparators [4]. The use of binary search for ADCs with more resolution will result in at least 100 samples per iteration needed per code edge measurement. Thus, this is not benefit in the test time of production testing. The servo-method is another method that utilizes a servo-circuit that does the function of a step search. This method is a fast hardware version which is very useful for production testing but it is not as fast as the histogram tests like linear ramp and sinusoidal methods [4]. In ADC testing, a histogram shows how many times each output code appears in the response vector, regardless the location [5]. Linear ramp simplifies computation due to the proportionality of the step width to the number of hits of each code [5–7]. But the speed of the ramp has not to be too fast unless the code will not be hit as many times as needed in order to get the best resolution and repeatability [8].

In this work, we choose to use the spectral analysis as a method of ADC characterization. Indeed, it is easier to produce a pure sinusoidal waveform than a perfectly linear ramp. This also allows to perform an improved characterization of dynamic performance of the ADC under test [4]. To achieve this goal, we designed and implemented an ADC characterization platform based upon a high performance data acquisition card and an analysis program using "Laboratory Virtual Instrument Engineering Workbench (LabVIEW)" programming environment. This analysis program provides all static and dynamic parameters of the ADC under test such as offset, gain, differential non-linearity (DNL) and integral non-linearity (INL) errors, signal-to-noise and distortion ratio (SINAD), spurious free dynamic range (SFDR) and the total harmonic distortion (THD). Furthermore, to manage uncertainties on the results given by our platform, we can define a datasheet associated with each converter tested. This datasheet indicates the set of uncertainties for each parameter (INL, DNL, SINAD, THD, etc.). The user of the converter would be able to take into account the uncertainty given in the datasheet. Moreover, it should be noted that manufacturers datasheets of ADCs provide only electrical characteristics, timing waveforms, timing diagrams, some applications, etc.

2 SAR conversion principle

The successive approximation ADC is by far the most popular architecture for data-acquisition applications, especially when multiple channels require input multiplexing. From the modular and hybrid devices of the 1970s to today's modern low-power ICs, the successive approximation ADC has been the workhorse of data-acquisition systems. The architecture was first utilized in experimental pulse-code-modulation systems by Bell Labs in the 1940s. Bernard Gordon, at Epsco, introduced the first commercial vacuum-tube SAR ADC in 1954; an 11-bit, 50-kSPS ADC that dissipated 500 W.[1]

The principle of the SAR consists of a sample-and-hold (S/H) circuit, a comparator, a DAC and a logic control unit. ADC employs a binary search algorithm that uses the digital logic circuitry to determine the value of each bit in a sequential or successive manner based on the outcome of the comparison between the outputs of the S/H circuit and DAC feedback from a capacitor array [9]. Figures 2 and 3 illustrate a block diagram of the SAR and the successive approximation conversion procedure, respectively [10].

Notice that four comparison periods are required for a 4-bit ADC. Generally, an *N*-bit SAR ADC requires *N* comparison periods and is not ready for the next conversion until all the bit values are determined. This explains why these ADCs are power and space efficient, yet are rarely seen in speed-and-resolution combinations beyond a few mega-samples per second (MSPS) at 14–16 bits. Some of the smallest ADCs available on the market are based on the SAR architecture [10].

In order to process rapidly changing signals, SAR ADCs have an input S/H to keep the signal constant during the conversion cycle. The conversion starts with the internal D/A converter set to midscale. The comparator determines whether the S/H output is greater or less than the DAC output, and the result (the MSB of the conversion) is stored in the SAR as a "1" or a "0". The DAC is then set either to 1/4 scale or 3/4 scale (depending on the value of the MSB), and the comparator makes the decision for the second bit of the conversion. The result ("1" or "0") is stored in the register, and the process continues until all the bit values are determined.

[1] http://www.analog.com/en/analog-dialogue/articles/the-right-adc-architecture.html.

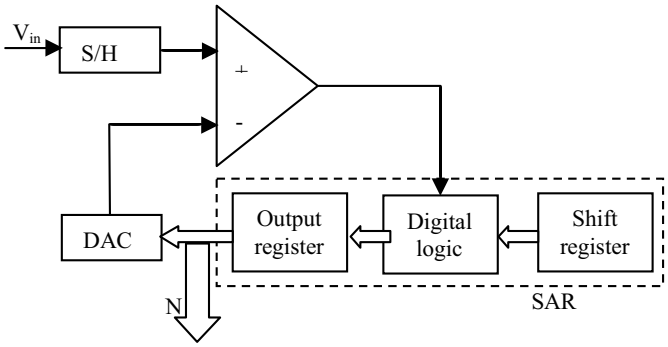

Fig. 2. Block diagram for the successive approximation register.

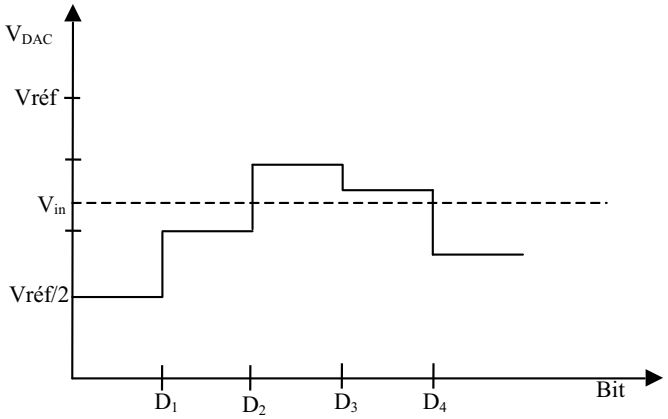

Fig. 3. 1.4-bit SAR ADC operation.

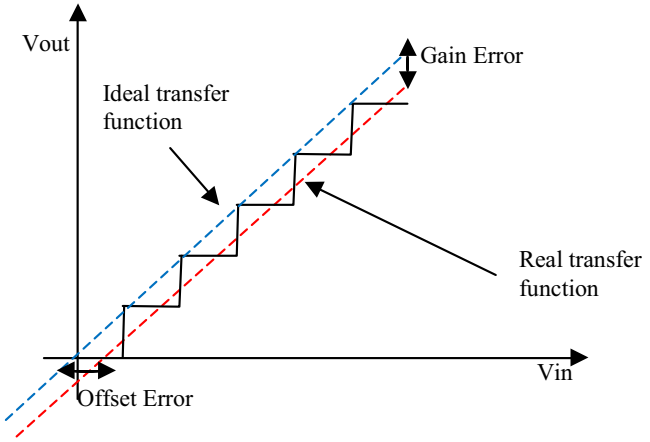

Fig. 4. Characteristics of non-ideal ADC.

3 Static and dynamic parameters

Traditionally, ADCs have been specified by their static characteristics such as INL and DNL, gain error and offset error. These specifications are important for determining the direct current (DC) accuracy of an ADC, and are very important in applications such as weighing, temperature measurement, and other situations where the input signal varies slowly over time.

Many applications, however, require digitizing a signal which varies quickly over time. These include digital signal processing (DSP) applications, such as digital audio, spectral analysis, and motion control. For these applications, DC accuracy is not as crucial as alternating current (AC) accuracy which is represented by the dynamic specifications, such as signal-to-noise ratio (SNR), THD, inter-modulation distortion (IMD), and SFDR. In this section, we present and discuss the various static and dynamic specifications used in the proposed characterization platform.

3.1 Static specifications

Due to limitations in elements used to fabricate an ADC on an integrated circuit (IC), manufactured ADCs have not perfect transfer functions. The deviations from perfect transfer functions define the dc-accuracy (static errors). Static errors affect the conversion of all input signals and can be fully characterized using non-varying input signals. Static errors are characterized by offset error, gain error, INL and DNL. Figure 4 illustrates some static specifications like:

- offset error: it is defined as the deviation of the actual ADC's transfer function from the perfect ADC's transfer function from zero to the measured transition [11];
- gain error: it represents the difference between ideal voltages which provides "full scale" output code versus the actual voltage for which the converter provides full scale output code [12];
- there are two major types of non-linearity that degrade the performance of an ADC: DNL and INL. The DNL is defined as the difference between an actual step width and the ideal value of 1LSB.[2] INL is the difference between the code centers from the ideal line [13]. INL can also be specified as the sum of DNLs [14]. DNL and INL equations are given by

$$\mathrm{DNL} = \frac{V_{D+1} - V_D}{V_{\mathrm{LSB-Ideal}} - 1}; \text{ where } 0 < D < 2^N - 1, \quad (2)$$

$$\mathrm{INL}_i = \sum_{j=0}^{i} \mathrm{DNL}_j, \quad (3)$$

where V_D is the electrical value corresponding to the digital output code D, N is the ADC resolution and $V_{\mathrm{LSB-Ideal}}$ is the ideal spacing for two adjacent digital codes[2];
- missing code: this situation occurs when a digital code at the ADC output is not produced for the corresponding input voltage [13].

3.2 Dynamic specifications

To obtain quantitative information on the dynamic performance of a converter, different specifications are defined, the most used of which are

- SNR is the ratio of the signal amplitude to the noise level (Eq. (4)). It is generally specified in the data sheets at a set of input signal frequencies, at a specific sampling rate,

[2] https://www.maximintegrated.com/en/app-notes/index.mvp/id/283.

and with the signal amplitude at or near the maximum allowable level [15]

$$\mathrm{SNR_{dB}} = 20\log\left(\frac{V_{\text{rms signal}}}{V_{\text{rms noise}}}\right), \tag{4}$$

where the lowercase characters "rms" means "root mean square".

A good estimation of the SNR value for a perfect N-bit converter excited by a full scale signal is given by [16]:

$$\mathrm{SNR_{dB}} = 6.02 \times N + 1.76. \tag{5}$$

– SINAD provides an information regarding the noise and harmonic energy present in the frequency spectrum. It is defined as:

$$\mathrm{SINAD} = \frac{\text{Fundamental input energy}}{\text{Summation of noise + distortion energy}}, \tag{6}$$

$$\mathrm{SINAD_{dB}} = 20 \times \log_{10}\left(\frac{S}{\sqrt{\sum_{f\neq f_{\text{in}}} S_i^2}}\right), \tag{7}$$

where S is the input signal effective value, and S_i, the effective value of the ith harmonic component [3].

– The effective number of bits (ENOB) is the number of bits with which the ADC behaves like a perfect ADC [11]. It is a widely used performance criteria and is derived from the formula of the SINAD:

$$\mathrm{ENOB} = \frac{\mathrm{SINAD} - 1.76}{6.02}. \tag{8}$$

– THD relates the "rms" sum of the amplitudes of the digitized signal harmonics to the amplitude of the signal:

$$\mathrm{THD} = \left(\frac{V_{f2}^2 + V_{f3}^2 + \cdots}{V_{f1}^2}\right)^{1/2}, \tag{9}$$

where V_{f1} is the amplitude of the fundamental and V_{fi} is the amplitude of the ith harmonic. To give an indication upon the harmonic distortion, particularly needed in the audio field, the THD is determined from the harmonic components H_k (k is an integer varying from 0 to user defined value) located at multiple frequencies of the input signal in the Nyquist band (from 0 to half the sampling frequency) [16]:

$$\mathrm{THD_{dB}} = 20 \times \log_{10}\left(\frac{\sqrt{\sum_k H_k^2}}{K}\right). \tag{10}$$

In practice, only the first few harmonics of the output signal are actually treated as distortion, while the remaining distortion is treated as noise. An ADC characterized by a low THD is especially important in applications such as audio and spectral analysis because in these applications, particularly, one does not want the conversion process to add new frequency components to the signal [3].

– The SFDR provides information regarding the difference between maximum amplitude tone in frequency spectrum and the fundamental input tone. It is defined as:

$$\mathrm{SFDR} = \frac{\text{Fundamental input energy}}{\text{Max (all frequency bins except fundamental)}}, \tag{11}$$

$$\mathrm{SFDR_{dB}} = 20 \times \log_{10}\left(\frac{\max(S_i)}{S}\right). \tag{12}$$

– IMD: this phenomenon occurs when two frequency components in a signal interact through the non-linearities in the ADC to produce signals at additional frequencies [15]. If f_1 and f_2 are the signal frequencies at the input of the device, the possible IMD products f_{12} are given by $f_{ab} = \mathrm{a}f_1 \pm bf_2$, where a and b are positive integer values, and are such that f_{12} is positive. The jth order IMD products are those for which $a + b = j$. IMD due to second order terms is commonly defined as:

$$\mathrm{IMD} = \left(\frac{V_{1,1}^2 + V_{1,-1}^2}{V_a^2 + V_b^2}\right)^{1/2}, \tag{13}$$

where V_a and V_b are the amplitudes of the fundamentals and $V_{1,1}$ and $V_{1,-1}$ are the amplitudes of the sum and difference frequencies, respectively.

4 Test hardware setup

4.1 Description of the proposed test platform

The hardware implementation of ADCs test setup, which is generally easy and fast, puts in evidence some difficulties due to the mixed nature of the tested component itself and the limitation of the test instrumentation. These difficulties increase with the speed and resolution of the ADC. The configuration of a classical test hardware is given in Figure 5.

A sinusoidal signal is used as input, a square signal is generally used to provide the clock that operates the ADC and a pulse generator for starting the conversion. The use of filters if often necessary for the clock, pulse and input signals to reduce noise and harmonic distortions. The mixed nature of ADCs requires coexisting on the same printed circuit board (PCB) three antagonistic elements: a sensitive analog part, a sensitive and noisy clock, and a noisy digital part. For these reasons, we proposed to optimize the test hardware by replacing the external instruments generating the test signals by some inputs/outputs (I/O) of an acquisition card. The latter is configured and controlled using a designed software. Figure 6 illustrates the proposed test hardware to characterize ADCs.

Through the proposed configuration, we are conform to IEEE Standard for Digitizing Waveform Recorders (IEEE Std. 1057) [17] and IEEE Standard for Terminology and

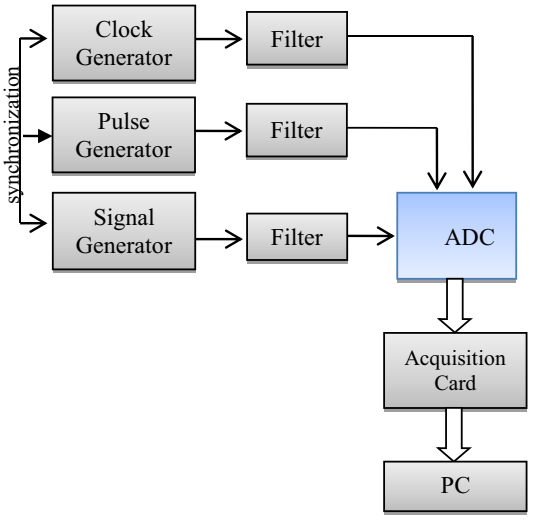

Fig. 5. Classical ADC test scheme.

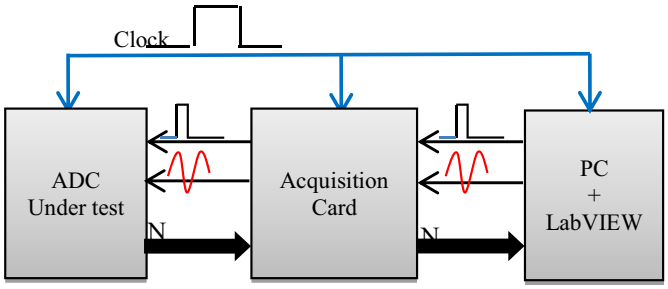

Fig. 6. Proposed ADC test setup.

Fig. 7. Implemented characterization platform.

Test Methods for Analog-to-Digital Converters (IEEE Std. 1241) [18] which specifies that the test setup should satisfy the following five conditions for accurately performing the spectral testing of ADCs. Firstly, the spectral purity of the input signal should be about 3–4 bits more pure than the ADC under test. In other words, to test an N-bit ADC, the input signal should be more than $N+3$ bits pure. The second condition is that the peak-to-peak voltage of the input signal should be slightly lower than the ADC input range so that the output of the ADC is not clipped. The third condition is to have very low relative jitter between the clock and input signals. The fourth condition is that, if possible, the input signal has to be coherently sampled. Finally, the total number of sampled points (or data record length) should be sufficiently large. Let F_{in} be the frequency of the input signal, F_c, the clock frequency, M, the total number of data points recorded to measure the spectral characteristics, and J, the total number of periods of the input signal sampled in the recorded data. The four parameters are related by the following equation:

$$J = \frac{MF_c}{F_{\text{in}}}. \tag{14}$$

With this configuration, we were able to reduce the effects of external noise from different instruments. In our case, a tested ADC receives firstly, a 100 ns pulse width to start conversion. Then, it receives an analog input signal from the personal computer (PC) via the I/O acquisition card. The amplitude of the input signal is selected such that its peak-to-peak value is within the ADC input range. The converter under test receives the analog signal and, after conversion, sends its digital output to PC. The latter will store these digital values to determine static and dynamic parameters. The input voltage and the pulse are generated from the designed configuration and control software of the acquisition card.

4.2 Characteristics of the proposed test platform

The proposed test platform is based upon the following parts:

- PCI 6052E is an acquisition card of National Instruments used to acquire digital data from the ADC under test. The digital data is send to the PC. The card has the following features [19]:
  - two 16-bit ADCs with 16 analog inputs,
  - 16-bit DACs with voltage outputs,
  - eight lines of transistor-transistor logic (TTL)-compatible DIO,
  - two 24-bit counter/timers for TIO;
- NI BNC-2110 is a connector block which simplifies the connection of analog signals, digital signals and timing I/O;
- a designed configuration and control application based on LabVIEW which is a system-design platform and development environment for a visual programming language from National Instruments;
- ADC 0804 is the ADC under test. It is a CMOS 8-bit, based on successive approximation A/D conversion method. It uses a differential potentiometric ladder similar to the 256R products [20].

The implemented characterization platform is presented in Figure 7. Figure 8 presents the LabVIEW interface developed to configure and control the acquisition card and also to perform the necessary calculation to obtain different static and dynamic characteristics.

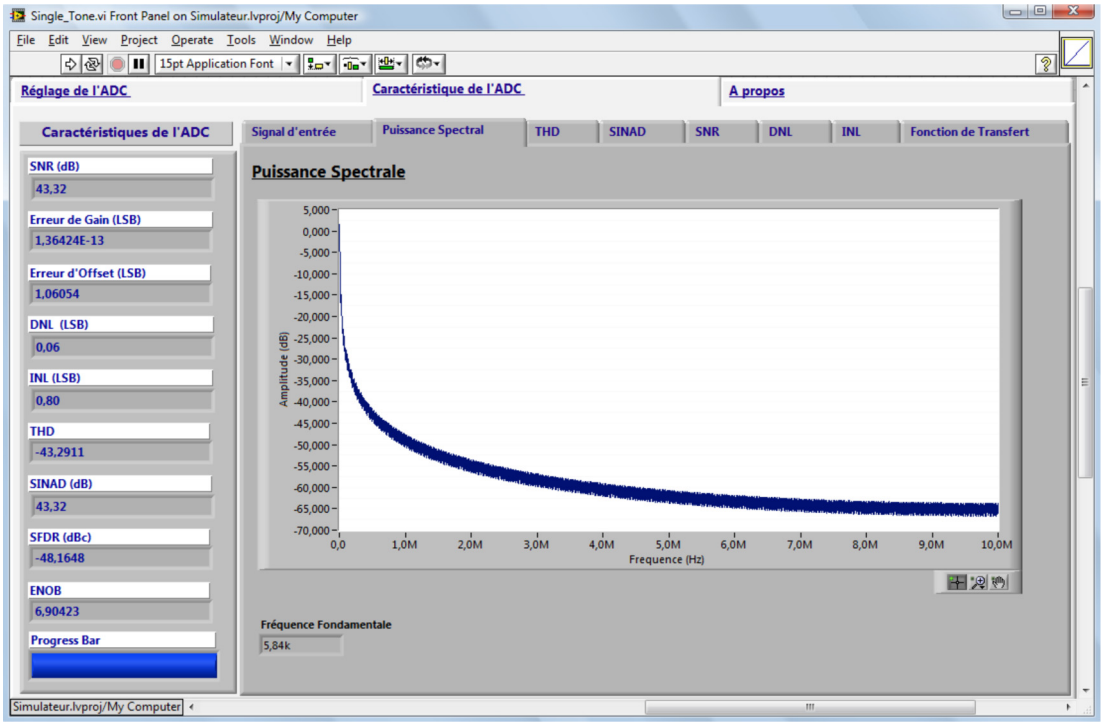

Fig. 8. The LabVIEW interface developed to configure and control the acquisition card and to perform the necessary calculation to obtain different static and dynamic characteristics.

Spectral analysis of the ADC is based on the exploitation of the Fourier transform of the digital samples acquired at the converter output when a pure sine wave is applied to its input. The resulting spectrum is analyzed to evaluate static and dynamic performances of the ADC. In the next section, an overview of spectral analysis will be presented.

Moreover, it should be noted that even if the PCI 6052E acquisition card is of an older generation, its characteristics are quite valid and sufficient for the application case that we have chosen. Our platform represents a prospective study applied to an ADC of average characteristics. We therefore used the acquisition card we have at the Research Laboratory "MMA-Lab" of INSAT-Tunis. It is also clear that improving the performance of our platform and testing converters of better characteristics requires the use of better performance acquisition cards such as the National Instruments PCI-6514 and PCI-6515.

5 Spectral analysis technique

A wide variety of tests have been developed to identify static and dynamic specifications. Many of these tests rely on Fourier analysis using the discrete Fourier transform (DFT) and the fast Fourier transform (FFT), as well as other mathematical models. The frequency domain tests extracts SFDR, THD, SINAD, SNR, and ENOB from the frequency spectrum of the ADC output response. In particular, the evaluation of the ADC performance is carried out by processing a DFT of a data record [21]. In frequency-domain methods, a sine wave is applied at the input of the ADC under test. Then, an appropriate algorithm chosen from those existing and based on the DFT of the corresponding ADC output codes is used to estimate the ADC dynamic parameters [16,22,23]. In fact, many algorithms are proposed in literature based on DFT and can be used to evaluate ADC dynamics parameters. Among these algorithms, we note "sine fitting" algorithms, commonly used in fast dynamic tests of ADCs. Traditionally they are used to measure noise, signal to noise and distortion ratio and ENOB. More recently they were proposed to obtain INL, DNL and the transfer function of ADCs, namely when they present a hysteric behavior. Also there are proposed algorithms for calculating in three steps, a near-optimum frequency "f_{nearopt}" which is close to any desired frequency. The signal parameters can also be determined using the maximum likelihood (ML) algorithm. The ML estimator is not influenced negatively by the (possibly) nonlinear characteristics of the ADC, thus the signal parameters, the fitting residuals and values such as SINAD, ENOB can be determined with the best achievable precision. Thus, we can evaluate the distortion and noise introduced by quantization [24].

Two spectral analysis techniques are commonly used:
– "single tone" technique;
– "dual tone" technique.

5.1 "Single tone" technique

The principle of this technique is to apply a pure sinusoidal input to the converter to perform the spectral analysis. Figure 9 shows an example of the spectrum obtained. We can observe the fundamental frequency of the input signal F_{in}, the harmonic frequencies kF_{in} (k is an integer value)

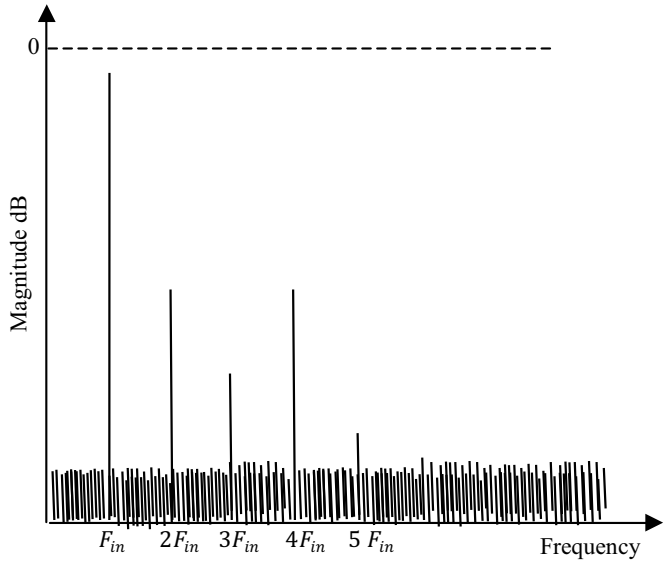

Fig. 9. "Single tone" spectral analysis (a theoretical illustration).

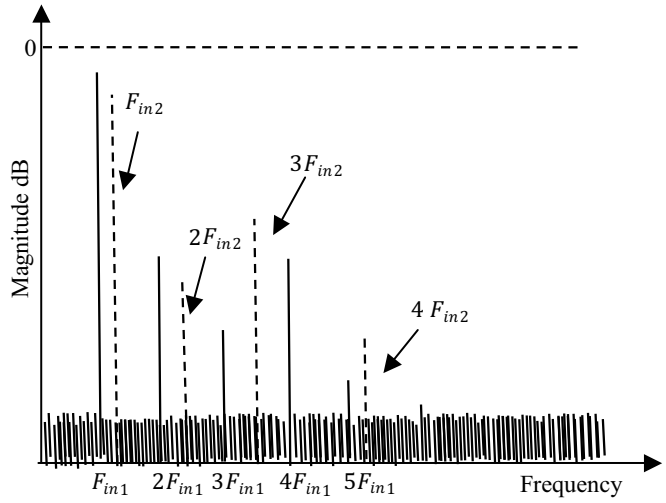

Fig. 10. "Dual tone" spectral analysis (a theoretical illustration).

and the noise created by the non-linearity of the converter [25]. This technique provides SINAD, THD, SFDR and the jitter of ADC.

5.2 "Dual tone" technique

"Dual tone" technique uses as input, the sum of two sinusoidal signals of frequency F_1 and F_2 having no harmonic relation between them ($F_1 \neq kF_2$, k is an integer). This technique allows highlighting all the phenomena of inter-modulation induced by the conversion of the composite signal [25]. IMD is generally caused by modulation, and it can occur when an ADC samples a signal composed of two (or multiple) sine-wave signals, F_1, F_2. IMD spectral components can occur at both the sum ($iF_1 + jF_2$) and the difference ($iF_1 - jF_2$) frequencies (i and j are integers) for all possible integer multiples of the fundamental (input frequency tone) or signal-group frequencies. Figure 10 shows an example of a spectrum

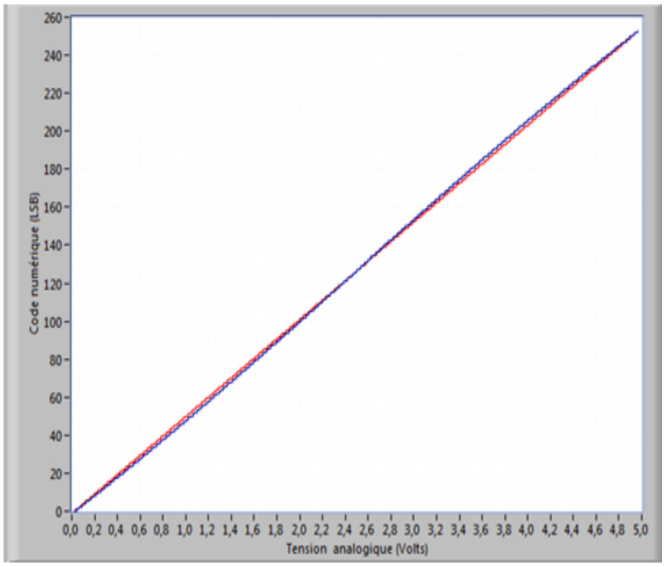

Fig. 11. Transfer functions of ADC under test and ideal ADC.

obtained with "dual tone" technique. We can observe the appearance of parasitic frequencies at $F_{ij} = iF_1 + jF_2$ in addition to the harmonic components of the input signal at frequencies $F_{k1k2} = k_1F_1 + k_2F_2$ (k_1 and k_2 are integers). These are the inter-modulation parasitic frequencies. With this testing technique, it is possible to determine the IMD of ADCs. In the next section, we will present the applied spectral analysis technique to identify and analyze the set of static and dynamic parameters of ADC.

It should be noted that for the scale of Figures 9 and 10, we have put on the x-axis F_{in}, $2F_{\text{in}}$, ..., and F_{in1}, $2F_{\text{in1}}$, ..., so, the scales depend on the values of F_{in} and F_{in1}. Indeed, these figures are theoretical and are given for illustration.

6 Static parameters evaluation

Static errors are due to the conversion of analog signals into digital signals (quantization error) and imperfections existing in a real ADC. "Single tone" technique is implemented on the successive approximation converter to identify static parameters of the "ADC 0804". Figure 11 shows the transfer function of the ADC under test (blue curve). This curve shows a slight deviation from the ideal transfer curve (red curve), this is due to the nonlinearity of the converter.

Using the same test, we determine the power spectral density "DSP" of the input signal, as shown in Figure 12. Then we identify the gain error, offset error, "INL" and "DNL". Figures 13 and 14 show the "DNL" and the "INL" of the ADC under test. In Table 1, the various static errors obtained by the "single tone" technique are summarized.

To highlight our experimental results of static test, we compared them to results obtained with the platform "CANTEST" [26]. The latter is a characterization system designed and developed in "Microelectronics IXL laboratory" in Bordeaux I University. It is used to characterize ADCs under test. It permits the evaluation of a set of parameters like SNR, INL, DNL, etc. There are many

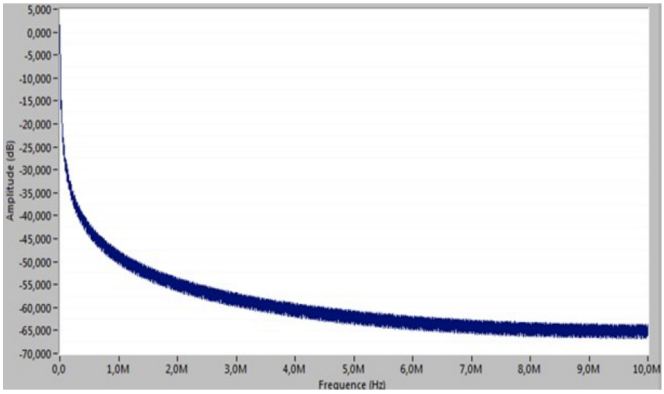

Fig. 12. Power spectral density of ADC under test.

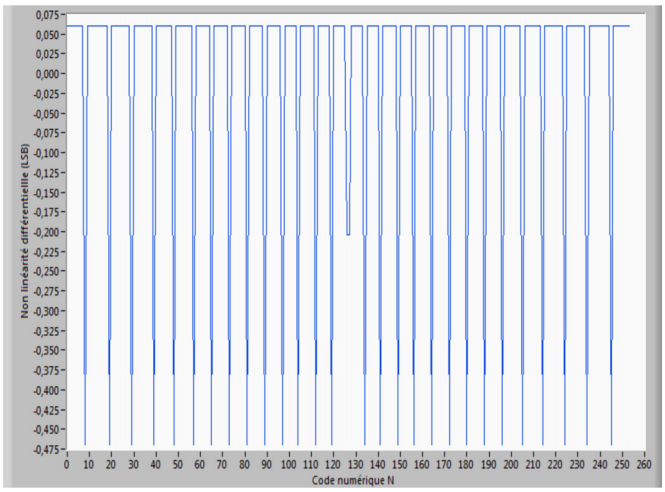

Fig. 13. Differential non-linearity of ADC under test.

versions of CANTEST: there is one developed with "C language" in "MAC" environment, an "ADCLab" version developed in Windows environment with "Matlab" and the newest version of CANTEST allows the use of logic analyzer HP16702 equipped with rapid acquisition probes HP16760. Table 2 compares the error rate differential and integral linearity obtained using the implemented platform and the results published for the CANTEST [27]. For the measurements of DNL errors, we note a slight difference between the two testing setup equals to 0.47 dB and 0.34 dB for INL measurements. Also, we notice a slight deviation between the rate of DNL and INL obtained by the two platforms, this is due to the error introduced by the last code (LSB). Indeed, the width of the first stage is 1/2LSB and the width of the last stage is 3/2LSB. Thus, the last code has the widest stage, hence the state transition can take place at different times with each acquisition. This allows influencing on the measurement results and implies possible errors on the measurement of DNL and INL. However, the test results showed good DNL and INL values and an acceptable correlation with the datasheet of the "ADC 0804" published by the manufacturer.

Furthermore, it has to be noted that the "ADC 0804"-type converter that we used can be provided by several sources, i.e., Intersil, National Instruments and Philips.

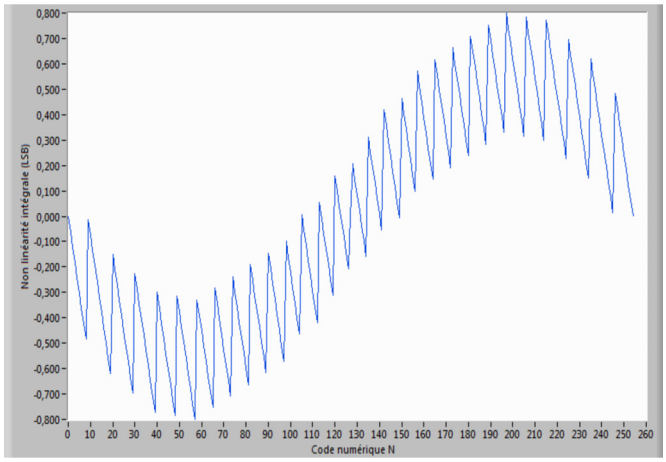

Fig. 14. Integral non-linearity of ADC under test.

Table 1. Test results obtained by spectral analysis.

Static parameters	Value
SNR [dB]	43.32
Gain error [LSB]	1.36E−13
Offset error [LSB]	1.06
DNL [LSB]	0.06
INL [LSB]	0.80
Missing codes	None

Unfortunately, developers of the platform CANTEST at Bordeaux I University have not indicated the manufacturer of the ADC that they used. On the other hand, we have taken care to consult various technical data sheets of suppliers and we considered that the declared deviations of the performances did not penalize for our work. So we decided to use the National Instruments ADC0804 circuit.

7 Dynamic parameters evaluation

We coupled the two testing techniques by spectral analysis in order to extract all of the dynamic parameters of the converter under test. We were able to determine the "THD", "SINAD", "SFDR", "ENOB" and "IMD". Table 3 shows the various errors obtained by the spectral analysis "dual tone" test. Figures 15 and 16 illustrate respectively the measurements of THD from the fundamental frequency to the 9th harmonic and IMD of the ADC under test.

Figure 15 gives the variation of THD versus frequency for the fundamental frequency and 8 successive harmonics. Values of those frequency peaks are little lower than fundamental peak. The second harmonic is located at $2\,\text{MHz} = 2 \times F_{\text{in}}$, the next at $3\,\text{MHz} = 3 \times F_{\text{in}}$, ..., the 9th harmonic is located at $9\,\text{MHz} = 9 \times F_{\text{in}}$. Figure 16 gives the variation of IMD versus frequency. Inter-modulation distortion is measured with two or more input signals at different, closely spaced frequencies, all of the same amplitude. We observe a fundamental peak equal to −52 dB and located at $1F_{\text{in}} = 1\,\text{MHz}$. IMD can be expressed

Table 2. Comparison between the results of measurements errors of differential and integral non-linearity.

	DNL [LSB]			INL [LSB]		
	Min	Max	ΔDNL	Min	Max	ΔINL
Implemented platform	−0.47	0.06	0.53	−0.79	0.80	−0.47
CANTEST	−0.81	0.19	1	−1.13	0.67	−0.81

Table 3. Measurements results of dynamic parameters by "dual tone" technique.

Dynamic parameters	Value
THD [dB]	−43.29
SINAD [dB]	43.32
ENOB [bits]	6.904
SFDR [dBFS]	−48.16
DFDR [dB]	−63.15
IMD [dB]	−49.89

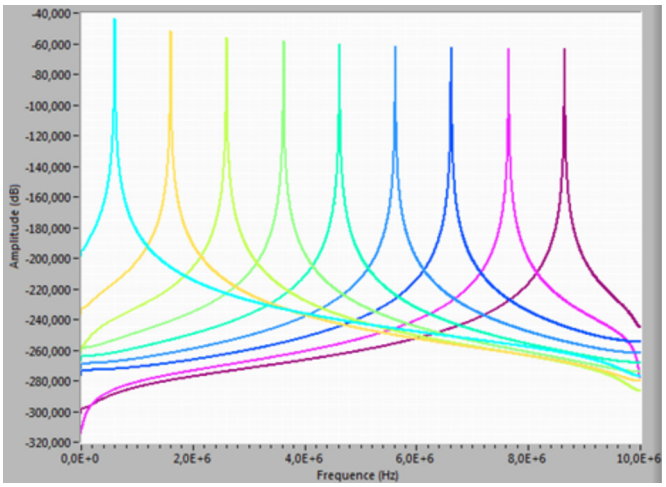

Fig. 15. Total harmonic distortion (THD) of ADC under test.

as the ratio of the power in the inter-modulation products to the power in one of the original input frequencies. Some applications, particularly those concerned with radio frequency signal processing, are more sensitive to some modulation products than others.

To highlight these results, we also compared the obtained measurements to another study made at Bordeaux I University [6]. Table 4 presents a comparison between results obtained using the implemented platform and the ones published in reference [6]. Through this table, we note a slight deviation between the two testing setup. For THD measurements, we found a difference equal to 1.23 dB, it represents 2.25% of the total THD value found in [6]. The overall obtained results show that the differences between the measurements and analysis results obtained using the implemented platform are very close to the published results in [6]. This is very encouraging in terms of overall performances of our platform.

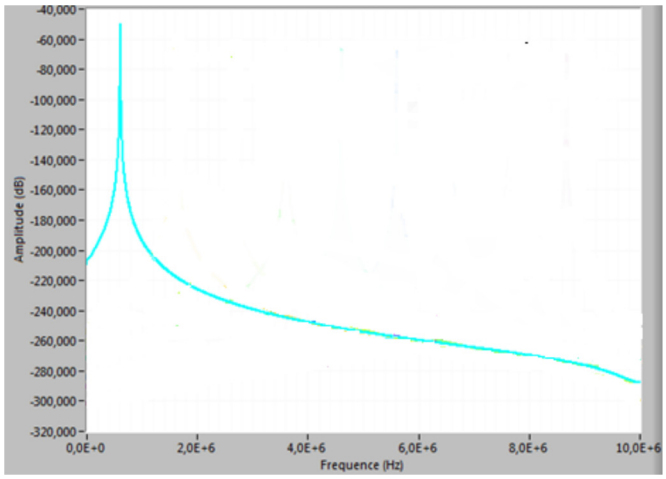

Fig. 16. Inter-modulation distortion (IMD) of ADC under test.

Table 4. Comparison of measurement results of dynamic parameters.

	Our results	[6]	ε
THD [dB]	−53.29	−54.52	1.23
SINAD [dB]	43.32	44.65	1.33
ENOB [bits]	6.90	7.60	0.66
IMD [dB]	−49.89	−55.92	6.03

8 Number of samples effects on static and dynamic specifications

The number of samples captured and processed by FFT for spectral analysis is a parameter of particular importance in a test environment. Indeed, the test time and material resources are directly dependent, they are the two main factors contributing to the overall test cost. Investigations have been performed by varying the number of samples N considered to perform the FFT. In this part of the study, we varied the number N of samples captured over the M acquisition periods which constitute the unitary test pattern. We scanned all the powers of 2 greater than $N_{\min} = 2^{10} = 1024$. With a coherent sampling, we provide a relationship between the sampling frequency F_s, the number of samples M, the test signal frequency F_{in} and the number of cycles in the sampled set J (see Eq. (14)). Thus, if the number of samples M is increased during a fixed

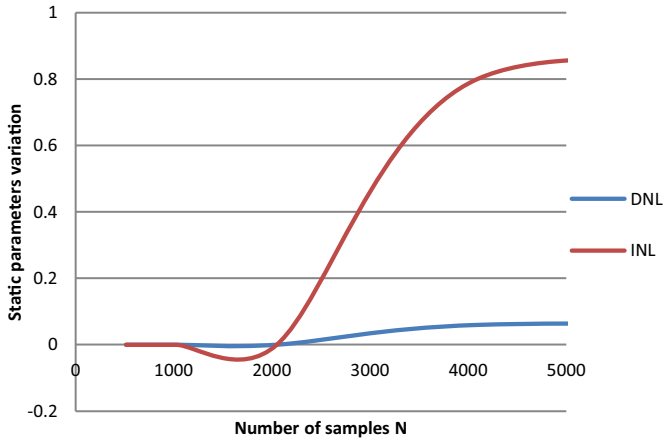

Fig. 17. Static parameters versus the number of samples.

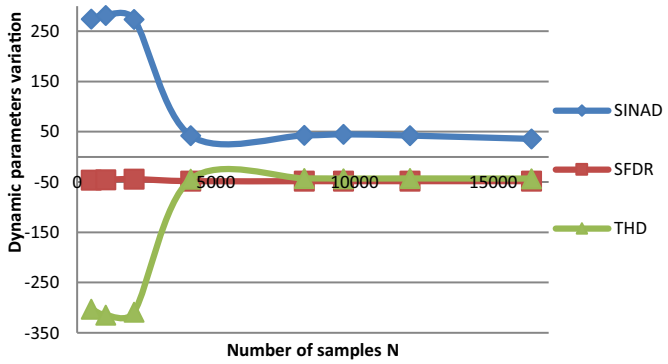

Fig. 18. Dynamic parameters versus the number of samples.

Table 5. Dispersion of static and dynamic parameters for $N = 4096$.

Static parameters	
$\varepsilon_{\mathrm{Nmin}}$ DNL	0.01%
$\varepsilon_{\mathrm{Nmin}}$ INL	0.01%
Dynamic parameters	
$\varepsilon_{\mathrm{Nmin}}$ SINAD	2.90%
$\varepsilon_{\mathrm{Nmin}}$ THD	2.21%
$\varepsilon_{\mathrm{Nmin}}$ SFDR	0.09%

number of periods of stimulus J, this increase raises the sampling period by keeping the frequency of the input signal F_{in} constant.

For illustration, Figures 17 and 18 give the variation of static (DNL and INL) and dynamic (SINAD, SFDR, THD) parameters versus the number of samples N. Unfortunately, we do not have theoretical values to perform a comparison with the experimental results. In fact, data sheet of the converter do not provide any static and dynamic specifications. It is important to mention that in our case "n", which is the number of ADC output bits (resolution), is equal to 8. As $N = 2^{n+4}$, the minimum value of N is $2^{8+4} = 2^{12} = 4096$; this is the minimum value of samples acquired to have a good accuracy for static and dynamic parameters measurement.

When a small number of samples is used for spectral analysis, it is clear that the values of the static and dynamic parameters measured are not the theoretically expected values in the case of a converter tested with the same signal amplitude. Moreover, we note that from the sample number N equal to 4096, the values of static and dynamic parameters vary slightly versus the number of samples. If we consider the dispersion of static and dynamic parameters when the number of samples taken into account is equal to its minimum value $N = 2^{n+4}$, we can meet the maximum measurement error $\varepsilon_{\mathrm{Nmin}}$ on each static and dynamic performance. The obtained results are compiled in Table 5. $\varepsilon_{\mathrm{Nmin}}$ represents the dispersion of static and dynamic parameters when the number of samples N equals to 4096. As an example, for INL measurement:

– for $N = 4096$, INL $= 0.8001$;
– for $N > 4096$, INL $= 0.8$

then $\varepsilon_{\mathrm{Nmin\ INL}} = [(0.8001 - 0.8)/0.8001] \times 100 = 0.01\%$.

The high value of dispersion is obtained for dynamic parameters: THD and SINAD, they are sensitive to the number of sample variations but in a tolerable range. These measurement errors are quite acceptable for the test.

One can notice that for spectral analysis, the sampling with a number $N = 4096$ of samples seems to separate two domains: under $N = 4096$: better accuracy on static measurement, and beyond $N = 4096$: better accuracy on the dynamic part. In fact, through Figures 17 and 18, we can observe a very low variation of static (INL, DNL) and dynamic (THD, SINAD, SFDR) parameters for $N \geq 4096$. For example, for INL measurements, we note a variation between -0.05 (LSB) and 0.82 (LSB) for $N < 4096$ and it is equal to 0.8 (LSB) for $N \geq 4096$. For SINAD measurement, we note a large deviation (250–32 dB) for $N < 4096$ and a small deviation (1%) for $N \geq 4096$. So, for static and dynamic parameters, to guarantee a better accuracy, we have to choose $N \geq 4096$. In general case, to ensure a high accuracy it is better to choose a number of samples greater than 2^{n+4}.

Furthermore, the study of amplitude effect on the measurements of static and dynamic parameters was performed. We have noted that static and dynamic parameters are sensitive to the variation of the amplitude of input signal. The maximum deviation of the SINAD and SFDR observed over the amplitude range studied (from $A = \mathrm{FS} - 5q$ to $A = \mathrm{FS} - q$, A: signal amplitude, FS: full scale, q: quantum) (Tab. 6) is small, in the order of 0.34 dB for SINAD and 1.48% for SFDR. So, the influence of the amplitude cannot induce more than 0.8% variation on the SINAD ratio and 3% on the SFDR ratio. For THD measurement, we have noted a large deviation equal to 10%. These results suggest that in the case of a real measurement of the dynamic parameters, any uncertainty on the amplitude of the input analog stimulus may lead to a significant measurement differences, especially for the measurement of THD.

9 Conclusion

In this paper, an experimental platform implemented for the characterization of ADCs is presented. The designed platform is a combination of hardware and software tools.

Table 6. Experimental results of the input signal amplitude variation influence on static and dynamic parameters [A: amplitude, FS: full scale, q: quantum].

	$A = \mathrm{FS} - 5q$	$A = \mathrm{FS} - 4q$	$A = \mathrm{FS} - 3q$	$A = \mathrm{FS} - 2q$	$A = \mathrm{FS} - q$	$A = \mathrm{FS}$
THD [dB]	−43.29	−44.19	−43.32	−45.22	−43.42	−41.11
SINAD [dB]	43.32	43.43	43.31	43.44	43.33	43.10
SFDR [dB]	−48.16	−49.17	−48.15	−49.24	−47.76	−48.46

The analysis technique used is the spectral analysis which is based upon FFT. This technique is commonly used in industry for analog and mixed signal circuits, especially ADCs. This technique consists of two complementary testing parts to identify all static and dynamic parameters of ADCs: gain error, offset error, INL, DNL, THD, SINAD, SFDR and IMD. The classical ADC0804 converter was used as a case study. The results obtained and compared to those achieved by the CANTEST experimental test system developed at Bordeaux I University (France) are very interesting and encouraging in terms of uncertainty and correlation. Moreover, many developments could be carried out with the validated platform but the most significant and immediate are the use of a more efficient acquisition card with a resolution up to 20 bits and the implementation of equivalent models of the converter under test in order to propose by simulation-optimization, for a possible redesign, some relevant physical modifications.

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